ABSTRACT OF THE DISCLOSURE

The present invention relates to a system and method for reducing the adverse impact of assertion instructions to processor performance so that programmers will be encouraged to include assertion instructions in computer programs. The system of the present invention includes memory and a compiler. The memory stores a first program to be compiled by the compiler. The compiler, in compiling the first program, translates a first function of the first program into a second function of a second program. The first function has assertion instructions that are translated by the compiler into translated assertion instructions, which are included in the second function. In compiling the first program, the compiler enables selective execution, based on a run time input, of a portion of the translated assertion instructions included in the second function.